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     (FILE 'HOME' ENTERED AT 10:19:10 ON 13 AUG 2002)
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          E ARNEY S/AU
L1      12 S E4,E7-9
          E BISHOP D/AU
L2     176 S E3,E13
          E BISHOP DAV/AU
L3      38 S E4,E16,E18
          E SHEA H/AU
L4      12 S E5,E10-11
L5       5 S L1-4 AND RELIAB?
L6  136726 S (CORROS? OR RUST OR MOISTURE OR HUMIDITY OR FAILURE OR RELIAB?)(6A)
          (SENSE# OR SENSING OR SENSOR OR DETECT? OR DETERMIN? OR TEST? OR
          ANALY? OR MEASUR? OR MONITOR? OR PREDICT? OR ESTIMAT? OR EVALUAT?)
L7     271 S L6 AND LEAK?(3A)CURRENT
L8     122 S (CORROS? OR RUST OR MOISTURE OR HUMIDITY) AND L7
L9     149 S L7 NOT L8
L10     42 S L9 AND (NOVEL OR KRYPTON OR DEFECT OR ASSESS? OR WAFER LEVEL)
L11   7493 S L6 AND (ELECTRODE OR MICROELECTRODE)
L12    101 S OXIDAT?(6A)(SENSE# OR SENSING OR SENSOR OR DETECT? OR DETERMIN? OR
          TEST? OR ANALY? OR MEASUR? OR MONITOR? OR PREDICT? OR ESTIMAT? OR
          EVALUAT?)AND L11
L13   1785 S LEAK?(3A)CURRENT(6A)(SENSE# OR SENSING OR SENSOR OR DETECT? OR
          DETERMIN? OR TEST? OR ANALY? OR MEASUR? OR MONITOR? OR PREDICT? OR
          ESTIMAT? OR EVALUAT? OR ASSAY? OR ASSESS?)
L14    122 S L6 AND L13
L15    310 S L5,L8,L10,L12,L14
L16    285 S L15 NOT PY>2000
L17     25 S L15 NOT L16
L18      2 S L17 AND(MEMS OR WAFER LEVEL)
L19    287 S L16,L18

=> d bib,ab l19 1-287

L19 ANSWER 2 OF 287  CA  COPYRIGHT 2002 ACS
AN   137:71044  CA
TI   Analysis TAT reduction by using emission-leakage failure analysis system
AU   Higuchi, Yasuhisa; Kawaguchi, Yasumasa; Sakazume, Tatsumi
CS   Device Development Center, Hitachi, Ltd., Ome, 198-8512, Japan
SO   Proceedings of ISSM2000, the International Symposium on Semiconductor
     Manufacturing, 9th, Tokyo, Japan, Sept. 26-28, 2000 (2000), 269-272
     Publisher: Ultra Clean Society, Tokyo, Japan.
AB   Current leakage is the major failure mode of semiconductor device
     characteristic failures. Conventionally, failures such as short circuit
     breaks and gate breakdowns were analyzed and the detected causes were
     reflected in the fabrication process. By using a wafer-level emission-
     leakage failure anal. method (in-line QC), the authors analyzed leakage
     mode failure, which is the major failure detected during the probe
     inspection process for LSIs, typically DRAMs and CMOS logic LSIs. The
     authors have thus developed a new technique that copes with the crit.
     structural failures and random failures that directly affect probe yields.

L19 ANSWER 3 OF 287  CA  COPYRIGHT 2002 ACS
AN   135:115052  CA
TI   A novel fast technique for detecting voiding damage in IC interconnects
AU   Foley, Sean; Floyd, Liam; Mathewson, Alan
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CS National Microelectronics Research Centre (NMRC), University College, Cork, Iran
SO IEEE International Reliability Physics Symposium Proceedings (1999), 37th, 213-220
AB A **novel** technique has been developed that is sensitive to the degree of voiding damage induced in a wide-line interconnect test structure. The technique is based on the measurement of the scattering parameters (S-parameters) of a simple, metal-line test structure over a range of high frequencies. The transmission-line parameter, G (leakage conductance), which is calcd. from the S-parameter measurements, is shown to be sensitive to distributed voiding, esp. in wider lines. This is significant for the following reasons: (1) the measurement is fast - a few seconds per test structure, (2) it can be performed at **wafer level**, (3) it does not rely on overstressing of the metalization and (4) it is sensitive to the amt. of voiding damage present in wide interconnect lines. Potential applications for this technique are: (a) an in-line statistical **reliability** control (SRC) **test** for the **detection** of stress voids induced during processing, and (b) an in-line SRC test for electromigration when preceded by a suitable current pre-stress step.

L19 ANSWER 5 OF 287 CA COPYRIGHT 2002 ACS
AN 135:100227 CA
TI Designing for **MEMS reliability**
AU **Arney, Susanne**
CS USA
SO MRS Bulletin (2001), 26(4), 296-299
AB This article provides a review of **MEMS reliability**-physics issues and **MEMS** specific test methodologies, failure modes, and solns. The examples emphasize electrostatically actuated **MEMS** and materials choices deriving from silicon or silicon-compatible fabrication techniques leveraged from the microelectronics industry. Solns. to **reliability** issues can be based on design, materials, or operational choices. **Reliability** concepts are potentially applicable over many **MEMS** device types, despite differences in materials choice, fabrication technique, or microelectromech. design.

L19 ANSWER 9 OF 287 CA COPYRIGHT 2002 ACS
AN 134:201389 CA
TI Anodic oxidation and **reliability** of MEMS poly-silicon electrodes at high voltages and in high relative humidity
AU **Shea, Herbert R.**; White, Carolyn D.; Gasparyan, Arman; Comizzoli, Robert B.; **Arney, Susanne**
CS Bell Labs, Lucent Technologies, Murray Hill, NJ, 07974, USA
SO Micro-Electro-Mechanical Systems (2000), 2, 345-348
AB We present a study of the anodic oxidn. of MEMS polysilicon electrodes and wires in ambients with high relative humidity and high voltages. MEMS poly-Si electrodes that are hermetically packaged in dry ambients show no signs of degrdn. on a time scale of years even when operated at hundreds of volts. To accelerate elec. failure modes, we expose unpackaged chips to ambients with high relative humidity. We then observe anodic oxidn. of the most pos. biased poly-Si structures on a time scale of minutes or hours. We describe this anodic oxidn. as a function of relative humidity and voltage, and its dependence on surface leakage currents.

L19 ANSWER 12 OF 287 CA COPYRIGHT 2002 ACS
AN 134:108939 CA
TI Electrical and environmental **reliability** characterization of surface-micromachined MEMS polysilicon **test** structures
AU White, Carolyn D.; **Shea, Herbert R.**; Cameron, Kimberly K.; Pardo, Flavio;

Bolle, Cristian A.; Aksyuk, Vladimir A.; **Arney, Susanne C.**
CS Lucent Technologies, Murray Hill, NJ, 07974, USA
SO Proceedings of SPIE-The International Society for Optical Engineering (2000), 4180(MEMS Reliability for Critical Applications), 91-95
AB While considerable press has been given to characterization of mech. properties of MicroElectroMech. Systems (MEMS) as related to **reliability**, environmental robustness, and lifetimes studies, characterization of elec. properties of MEMS have not been widely published. In this paper we present an examn. of elec. properties (surface and substrate **leakage currents**, sheet resistance, substrate contact resistance and interlayer contact resistances) of polysilicon thin films used in surface micromachined MEMS test structures. Environmental and elec. overstress conditions that affect leakage have been studied. Two test structures have been used to independently study surface and substrate **leakage currents** at different levels of **humidity** (0% to 80% RH) and applied voltage (100 to 150 V). Both static and lifetime studies have been conducted. Significant differences in surface and substrate leakage lifetime characteristics are obsd., suggesting different failure mechanisms for these two important elec. phenomena in MEMS **reliability**.

Also look at U3880

L19 ANSWER 13 OF 287 CA COPYRIGHT 2002 ACS
AN 134:93843 CA
TI Anodic oxidation and **reliability** of MEMS polysilicon electrodes at high relative humidity and high voltages
AU **Shea, Herbert R.**; Gasparyan, Arman; White, Carolyn D.; Comizzoli, Robert B.; Abusch-Magder, David; **Arney, Susanne C.**
CS Bell Laboratories, Lucent Technologies, Murray Hill, NJ, 07974, USA
SO Proceedings of SPIE-The International Society for Optical Engineering (2000), 4180(MEMS Reliability for Critical Applications), 117-122
AB The authors present a full factorial study of the effect of relative humidity and voltage on the oxidn. of surface-micromachined poly-silicon wiring and electrodes. The system consists of 500 nm thick poly-Si wires and electrodes insulated from the substrate wafer by 600 nm of Si-rich SixNy, fabricated using a surface-micromachining process. In dry ambients, oxidn. or damage to the bottom poly-Si layer in MicroElectroMech. Systems (MEMS) devices occurs so slowly that little can be learned in a timely manner, even when stressing the electrodes at elec. fields close to dielec. breakdown. We observe however that in ambient with elevated relative humidity the wires and electrodes anodically oxidize within a short period of time when operated at moderately large voltages. Only the most pos. biased poly-Si structures oxidize, and we describe the anodic oxidn. and assocn. vol. expansion as a function of a no. of accelerating factors including relative humidity and voltage. A threshold is obsd. in relative humidity bot not in voltage.

TR165, p54

L19 ANSWER 17 OF 287 CA COPYRIGHT 2002 ACS
AN 133:259944 CA
TI **Analysis** of **leakage currents** and impact on off-state power consumption for CMOS technology in the 100-nm regime
AU Henson, W. Kirklen; Yang, Nian; Kubicek, Stefan; Vogel, Eric M.; Wortman, Jimmie J.; De Meyer, Kristen; Naem, Abdalla
CS Interuniversity Micro-Electronics Center, Louvain, 3001, Belg.
SO IEEE Transactions on Electron Devices (2000), 47(7), 1393-1400
AB Off-state leakage currents have been investigated for sub-100 nm CMOS technol. The two leakage mechanisms investigated in this work include conventional off-state leakage due to short channel effects and gate leakage through ultrathin gate oxides. The conventional off-state leakage due to short channel effects exhibited the similar characteristics as

previously published; however, gate leakage introduces two significant consequences with respect to off-state power consumption: (1) an increase in the no. of transistors contributing to the total off-state power consumption of the chip and (2) an increase in the conventional off-state current due to gate leakage near the drain region of the device. By using exptl. measured data, it is estd. that gate leakage does not exceed the off-state specifications of the National Technol. Roadmap for Semiconductors for gate oxides as thin as 1.4 to 1.5 nm for high-performance CMOS. Low power and memory applications may be limited to an oxide thickness of 1.8 to 2.0 nm in order to minimize the off-state power consumption and maintain an acceptable level of charge retention. The **anal.** in this work suggests that **reliability** will probably limit silicon oxide scaling for high-performance applications whereas gate leakage will limit gate oxide scaling for low power and memory applications.

L19 ANSWER 18 OF 287 CA COPYRIGHT 2002 ACS
AN 133:201310 CA
TI Characterization of gate dielectrics with mercury gate MOS current-voltage measurements
AU Gruber, Gilbert A.; Hillard, Robert J.
CS Solid State Measurements, Inc., Pittsburgh, PA, 15275, USA
SO ASTM Special Technical Publication (2000), STP 1382(Gate Dielectric Integrity), 65-73
AB MOS device performance and reliability depend strongly on the quality of the gate dielec. Metallic contamination, stoichiometry, interface properties, and substrate quality all have an influence. Gate Oxide Integrity (GOI) measurements are frequently used for **monitoring** oxide quality and **reliability**. Conventionally, testing the integrity of these gate dielecs. requires the use of prefabricated polysilicon or metal gate MOS capacitors (MOSCAPs). However, this involves short loop processing that is time-consuming and can itself affect the gate oxide quality. Therefore, a method that can monitor these factors rapidly and accurately for both prodn. and process development is highly desirable. In this paper, a mercury gate is presented for Gate Oxide Integrity (GOI) measurements. This mercury gate is formed using a highly repeatable mercury probe Capacitance-Voltage/Charge-Voltage/Current-Voltage (CV/QV/IV) system. Several applications are discussed that show how these measurements may be used in monitoring a variety of process-induced **defects**. An example of the application of mercury gate Metal-Oxide-Semiconductor Current-Voltage (MOS IV) measurements for ultrathin (less than 10 nm) oxide development is also presented.

L19 ANSWER 21 OF 287 CA COPYRIGHT 2002 ACS
AN 133:97492 CA
TI Reliability: a possible showstopper for oxide thickness scaling?
AU Degraeve, Robin; Kaczer, Ben; Groeseneken, Guido
CS IMEC, Louvain, 3001, Belg.
SO Semiconductor Science and Technology (2000), 15(5), 436-444
AB Gate oxide reliability is an essential factor in qualifying CMOS technologies. An accurate and consistent methodol. for **detg**. ultrathin oxide **reliability** is therefore needed. In this paper, the crucial steps of this methodol. are analyzed. First it is demonstrated that soft and hard breakdown show an identical distribution and therefore extrapolation, from the test voltage to a voltage where the soft to hard breakdown prevalence ratio is different, is allowed. Secondly, the log-normal distribution is shown to be inadequate to describe the tBD-statistics; only the Weibull distribution can be used. Thirdly, based on stress-induced **leakage current measurements**, it is concluded that a ln(tBD)-Vg-dependence is well suited

to extrapolate high voltage tBD-data to low voltage. It is demonstrated that in the 1 to 2 V range, the gate voltage shows no threshold value below which the oxide degrdn. is reduced or altered. A detailed anal. in the oxide thickness range 2 to 5 nm is presented showing that oxide reliability might become a major showstopper for the further downscaling of CMOS technol. Possible flaws in the **reliability prediction** methodol. are discussed and guidelines for future research are indicated.

L19 ANSWER 26 OF 287 CA COPYRIGHT 2002 ACS
AN 132:215210 CA
TI MOCVD TiN diffusion barriers for copper interconnects
AU Choe, H. S.; Danek, M.
CS Novellus Systems, Inc., San Jose, CA, 95134, USA
SO IEEE International Interconnect Technology Conference, Proceedings, San Francisco, May 24-26, 1999 (1999), 62-64 Publisher: Institute of Electrical and Electronics Engineers, New York, N. Y.
AB Copper barrier effectiveness of ultrathin 100-Å MOCVD titanium nitride (TiN) and silane-treated titanium nitride [TiN(Si)] films was investigated and compared to that of the industry std. 150-Å PVD Ta barrier. The metallurgical stability of the film and barrier **failure** was **detd.** by sheet resistance change, optical and electron microscopy after Secco etch and C-V measurements. Copper drift through the barrier was tested under bias temp. stress conditions (200° and 2 MV/cm) using **leakage current** vs. time **measurements** on MOS capacitors.

L19 ANSWER 27 OF 287 CA COPYRIGHT 2002 ACS
AN 132:188296 CA
TI Reliability characterization of **moisture**-induced degradation of low-k dielectric behavior for advanced interconnects
AU Ionescu, A. M.; Mondon, F.; Blachier, D.; Morand, Y.; Reimbold, G.
CS LETI (CEA-Direction Technologies Avancees), Grenoble, 38054, Fr.
SO Materials Research Society Symposium Proceedings (1999), 565(Low-Dielectric Constant Materials V), 101-106
AB This paper reports degrdn. characteristics of low-k dielec. (FOX) in multilevel metal structures (comb-type capacitors) submitted to **moisture** stress. A large increase of **leakage current** (>105) and capacitance (up to x3) is obsd. after **moisture** stress when only FOX is used as lateral dielec., while moderate degrdn. takes place when an oxide liner is placed between FOX and metal lines. Enhanced **moisture** induced degrdn. is found on previously probed dices with respect to virgin devices. Systematic elec. measurements, combined with SEM **anal.**, are performed to find out the **moisture** diffusion path. When contact pads are damaged by previous probing (owing to the mech. weakness of FOX in the pad stack), they provide a direct entry path for enhanced **humidity** intake. **Humidity** is also shown to enter through wafer border. Using a SiO2 liner combined with FOX improves considerably the resistance to **moisture** degrdn.

L19 ANSWER 30 OF 287 CA COPYRIGHT 2002 ACS
AN 132:99512 CA
TI Passivation and **corrosion** of microelectrode arrays
AU Schmitt, G.; Fassbender, F.; Luth, H.; Schoning, M. J.; Schultze, J.-W.; Buss, G.
CS Laboratory Corrosion Protection, Iserlohn Univ. Applied Sciences, Iserlohn, D-58644, Germany
SO Materials and Corrosion (2000), 51(1), 20-25
AB The application of Si based microsensors in aq. environments is hindered by unsatisfactory barrier properties and poor **corrosion** resistance of common passivation layers which give insufficient protection to electronic

microstructures. Investigations of the protective effect of various types of layers (compatible to Si planar technol.) against 1 M NaCl at pH 2-10 are described. **Failures** of the passivation layers were **detected** by **leak current** and cond. **measurements** with subsequent investigations of **failure** mechanisms by SEM. Both org. and inorg. films were tested with chips which were completely covered with the passivation layer. Org. films had a time to failure of at best 500 h, achieved by Probimer and plasma treated polyimide. The poor barrier properties of PECVD-SiO2 and Si3N4 monolayers (only a few hours) were clearly surpassed by combining the monolayers to SiO2/Si3N4-duplex and SiO2/Si3N4/SiO2 triplex (ONO) layers. The most promising barrier properties were achieved by the triplex (ONO) layer which yielded a time to failure of 1200 h compared to 500 h for the duplex layer on non-buried conducting tracks. Burying the conducting tracks into the thermal SiO2 layer significantly improved the performance of the duplex (2000 h) and the SiC layer (1000 h compared to 700 h on non-buried tracks) once again. In the case of open electrodes the Si3N4 layer quickly failed, whereas the duplex and the SiC layer revealed better protective properties. Org. films failed due to swelling and the formation of blisters. Intrinsic mech. stress with chem. interaction resulted in stress **corrosion** cracking (SCC) and finally lead to the failure of the inorg. PECVD layers.

L19 ANSWER 31 OF 287 CA COPYRIGHT 2002 ACS
AN 132:7970 CA
TI High reliability plastic packaging for microelectronics
AU Sweet, James N.; Peterson, David W.; Hsia, Alex H.; Tuck, Melanie
CS Advanced Packaging Department, Sandia National Laboratories, Albuquerque, NM, 87185-1082, USA
SO Sandia National Laboratories [Technical Report] SAND (1997), SAND97-1721, 1-35
AB This Lab. Directed Research and Development (LDRD) project conducted in fiscal years 1996 and 1997 under case 3526.030 was devoted to the development of test structures and assocd. **measurement** methodol. for assessing the **reliability** of plastic encapsulated microelectronic devices. The end goal was the conceptual specification of one or more Assembly Test Chips (ATCs) which could be used evaluating plastic encapsulation technologies. In this work the authors demonstrated suitable circuits for **measuring** Au-Al wirebond and Al metal **corrosion failure** rates during accelerated temp. and **humidity testing**. Also the test circuits on the authors' ATC02.5 chip were very sensitive to extrinsic or processing induced failure rates. A no. of accelerated aging expts. were conducted with unpassivated triple track Al structures on the ATC02.6 chip to demonstrate that these would be extremely sensitive to environmental conditions. The authors found an unexpected result, the unpassivated tracks were very sensitive to particulate contamination which caused conductor damage and resultant high voltage breakdown. A no. of modifications to existing circuity were suggested as a result of the unpassivated device expts. Also the piezoresistive stress sensing circuitry which the authors had designed for the ATC04 test chip was suitable for detg. the change in the state of mech. stress at the die when both initial and final measurements were made near room temp. However, the authors' attempt to measure thermal stress between room temp. and a typical polymer glass transition temp. failed because of excessive die resistor-substrate breakage currents at the high temp. end. Suitable circuitry changes were developed which should eliminate this problem. One temp. and **humidity** expt. was conducted with Sandia developed static random access memory (SRAM) parts to examine non-**corrosion** CMOS failures. This expt. did not achieve the desired objective because of processing problems but the authors did demonstrate that the authors could easily **detect** and **measure** a

new type of **corrosion failure** mode, this time at the model to Si contacts on the die surface. As a result of this two year effort, the authors have new designs for a no. of test circuits which could be used on an advanced ATC for reliability assessment in Defense Programs electronics development projects.

L19 ANSWER 36 OF 287 CA COPYRIGHT 2002 ACS
AN 131:162516 CA
TI Passivation and **corrosion** of microelectrode arrays
AU Schmitt, G.; Schultze, J.-W.; Fassbender, F.; Buss, G.; Luth, H.; Schoning, M. J.
CS Laboratory for Corrosion Protection, Iserlohn University of Applied Science, Iserlohn, 58590, Germany
SO Electrochimica Acta (1999), 44(21-22), 3865-3883
AB A review with 64 refs. concerning passivation and **corrosion** of microelectrode arrays is presented. Application of silicon based microsensors in electrolyte solns. is hampered by insufficient barrier properties and poor **corrosion** resistance of common passivation layers used to protect the underlying conducting tracks and microelectronic structures. Therefore, the protectivity of various types of compatible passivation layers (org. polyimide and photoresist films, inorg. mono, duplex and triplex layers based on PECVD silicon oxide and silicon nitride) was investigated and improved on microelectrode arrays exposed to 1 M NaCl (pH 2 to 10) at 25°C. Duplex SiO2/Si3N4 and oxide/nitride/oxide (ONO) triplex layers with optimized nitride PECVD process yielded the best barrier properties. Burying the conducting tracks in the thermal silicon oxide layer improves the performance significantly. **Failures** of the passivation layers, **detected** by **leak current** and layer resistance **measurements** with subsequent SEM investigation, result from cracking due to intrinsic and extrinsic (less important) mech. stress, film defects (pinholes, particle inclusions), from chem., physicochem. and electrochem. reactions (external, internal, sublayer **corrosion**) and from the combined action of mech. stress and chem. interaction (stress **corrosion** cracking).

L19 ANSWER 43 OF 287 CA COPYRIGHT 2002 ACS
AN 130:319074 CA
TI Electric field and temperature acceleration of quasi-breakdown phenomena in ultrathin oxides
AU Roy, D.; Bruyere, S.; Vincent, E.; Ghibaudo, G.
CS STMicroelectronics, Central R and D Labs, Crolles, 38926, Fr.
SO IEEE International Integrated Reliability Workshop Final Report, Lake Tahoe, Calif., Oct. 12-15, 1998 (1998), 49-54 Publisher: Institute of Electrical and Electronics Engineers, New York, N. Y.
AB The quasi-breakdown phenomenon is studied for 3.5-nm ultrathin gate oxides. The appearance of this failure mode is studied and the assocd. **leakage current** is characterized. Also, the elec. field and temp. dependences of the quasi-breakdown occurrence are analyzed: a **novel** procedure is proposed to det. the assocd. acceleration and to be able to **predict** the **reliability** with respect to this **failure** mode under nominal use conditions for deep-submicron technologies. The quasi-breakdown phenomenon is a major limiting factor for ultrathin oxide reliability.

L19 ANSWER 45 OF 287 CA COPYRIGHT 2002 ACS
AN 130:190404 CA
TI A comparison between the DC **leakage currents** of polymer housed metal oxide surge arresters in very humid ambient conditions and in water immersion tests
AU Lahti, K.; Kannus, K.; Nousiainen, K.

CS Tampere University of Technology Power Engineering, Tampere, FIN-33101, Finland
SO IEEE Transactions on Power Delivery (1999), 14(1), 163-168
AB The behavior of **leakage currents** of seven different types of com. available polymer housed metal oxide surge arresters was studied in very humid ambient conditions during a 16 mo test. During the test series many different combinations of mech., elec. and **humidity** stresses were applied to the **test** specimens to obtain the range of **leakage current** behavior possible for the different arrester types in humid ambient conditions. The **leakage current** behaviors **measured** for the different arrester types are compared to their behavior in the boiling H2O immersion test. This wide comparison gives valuable information of possible **leakage current** behaviors of several modern arrester types in humid ambient conditions and esp. of the suitability of the boiling H2O immersion test for sealing testing of polymer housed arrester types. In general, both tests revealed the same kinds of d.c. **leakage current** behavior in the different arrester types although some effects of different arrester structures and H2O penetration phenomena were obsd.

L19 ANSWER 54 OF 287 CA COPYRIGHT 2002 ACS
AN 130:19329 CA
TI Long-term **reliability evaluation** of power semiconductor devices used in substation rectifiers
AU Horiuchi, Toshikazu; Sugawara, Yoshitaka
CS Technical Research Center of The Kansai Electric Power Co., Inc., Amagasaki city, 661-0974, Japan
SO Proceedings of the International Symposium on Power Semiconductor Devices & ICs, 10th, Kyoto, June 3-6, 1998 (1998), 195-198 Publisher: Institute of Electrical Engineers of Japan, Tokyo, Japan.
AB To enable **evaluation** of the long-term **reliability** of power semiconductor devices used in com. substations, this paper presents the failure rate of such devices in practical use. Recovery activation energies are also evaluated from annealing and bias stress test. Degraded devices are disassembled and examd. In some of them, melting and **defect** of Si chip edge caused large **leakage current**. Also **leakage current** spectrum is strongly related to breakdown voltage degrdn. A **novel monitoring** method using **leakage current** spectrum is proposed here for the 1st time.

L19 ANSWER 59 OF 287 CA COPYRIGHT 2002 ACS
AN 129:304099 CA
TI Quartz-oscillator **humidity sensor** elements with anodic-**oxidation** coatings
IN Ue, Makoto; Mizutani, Bunichi; Takeuchi, Sachie
PA Mitsubishi Chemical Industries Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 4 pp.
PI JP 10253519 A2 19980925 JP 1997-53027 19970307
AB The title elements are composed of a quartz resonator made of **electrode** metal film(e.g., Al), quartz plate, and **electrode** metal film, and anodic-**oxidn**. coatings as **moisture-sensing** coatings formed on the **electrode** metal films with nonaq. chem. conversion solns. contg. ≤5 wt.% H2O.

L19 ANSWER 67 OF 287 CA COPYRIGHT 2002 ACS
AN 129:114753 CA
TI **Corrosion** rate **measurements** by non-linear electrochemical impedance spectroscopy. Comments on the paper by K. Darowicki, Corros. Sci. 37, 913 (1995)
AU Diard, J. -P.; Le Gorrec, B.; Montella, C.
CS Laboratoire d'Electrochimie et de Physicochimie des Materiaux et Interfaces, Ecole Nationale Superieure d'Electrochimie et

d'Electrometallurgie de Grenoble, UMR 5631 CNRS-INPG, associe a l'UJF, Saint Martin d'Heres, 38402, Fr.
SO Corrosion Science (1998), 40(2/3), 495-508
AB The **detn.** of **corrosion** parameters from the exptl. dependence of the non-linear polarization resistance of corroding **electrodes** on the amplitude of sinusoidal modulation of the **electrode** potential has been proposed in the literature, by using a theor. expression which takes the influence of electrolyte resistance into consideration. It is shown that this expression is only valid for low amplitudes of the perturbation signal, neglecting the influence of the ohmic drop. Moreover, if the electrolyte resistance is non-negligible and no IR compensation is carried out exptl., this theor. expression is incorrect, leading to erroneous values for the corrosion parameters. An alternative method is proposed, based on numerical calcn. of the non-linear polarization resistance.

L19 ANSWER 69 OF 287 CA COPYRIGHT 2002 ACS
AN 128:302577 CA
TI Behavior of the d.c. **leakage currents** of polymeric metal oxide surge arresters in water penetration tests
AU Lahti, K.; Kannus, K.; Nousiainen, K.
CS Tampere University of Technology Power Engineering, Tampere, FIN-33101, Finland
SO IEEE Transactions on Power Delivery (1998), 13(2), 459-464
AB The behavior of seven com. available polymer housed metal oxide surge arrester types was studied in +70°C and boiling water immersion tests. D.c.**leakage current** of the arresters was used to diagnose the **humidity** penetration inside an arrester. The recovery features after an immersion test for different arrester types were measured and discussed. Together with the immersion and recovery **tests** a **humidity** penetration **test** in very humid air was performed. For the first time the behavior of different arrester types in immersion tests was compared to their behavior in a **humidity** penetration **test** with realistic ambient conditions. The resistance to **moisture** penetration varied greatly in the arrester types tested. Also recovery of the DC **leakage current** varied between the arrester types depending on their structure. The results from the tests in very humid air indicated similar arrester behaviors than the results from the other tests and suggest ideas for diagnosing arrester behavior.

L19 ANSWER 71 OF 287 CA COPYRIGHT 2002 ACS
AN 128:96311 CA
TI **Reliability evaluation** of low k dielectric materials for sub-micron interconnection application
AU Nguyen, D.; Mcgahay, V.; Endicott, G.; Agarwala, B.; Rathore, H.; Yankee, S.
CS IBM Microelectronics, Semiconductor Research and Development Center, Hopewell Jct., NY, 12533, USA
SO Proceedings - Electrochemical Society (1997), 97-8(Low and High Dielectric Constant Materials: Materials Science, Processing, and Reliability Issues), 112-125
AB A study was carried out on various oxides to replace the current PECVD SiO2 deposition/etch/deposition process by studying alternative insulators with different deposition techniques such as high d. plasma (HDP) oxide, fluorinated Si glass (FSG) oxide, H silsesquioxane spin-on dielec. or low k flowable oxide (FOx). The objectives of a suitable insulator are good gap fill capability, low dielec. const., and low defect d. and reliable. A no. of **reliability tests** were carried out to **evaluate** the performance and the **reliability** of films by using SEM cross sections for gap fill verification, dielec. const. **measurements**, I-V **leakage current measurements**, Interlevel

Dielec. (ILD) step voltage ramp test, time dependent dielec. breakdown (TDDB) stress, electromigration, stress migration, thermal cycling and **corrosion tests**. In summary, stress data indicated that FOx is the best insulator to replace PECVD oxide for future deep-submicron BEOL applications. For the purpose of good gap filling, HDP Oxide is a suitable insulator for a replacement of PECVD oxide dep./etch process.

L19 ANSWER 72 OF 287 CA COPYRIGHT 2002 ACS
AN 128:89689 CA
TI **Corrosion** from combustion products - an overview
AU Gandhi, Pravinray D.
CS Underwriters Laboratories Inc., Northbrook, IL, 66062, USA
SO Meeting of the UJNR Panel on Fire Research and Safety, 13th, Gaithersburg, Md., Mar. 13-20, 1996 (1997), Meeting Date 1996, Volume 1, 209-224. Editor(s): Beall, Kellie Ann. Publisher: National Institute of Standards and Technology, Gaithersburg, Md.
AB There has been a keen focus to understand **corrosion** from combustion products as it is related to potential damage from their deposition on equipment. Several test methods are available to assess the potential for **corrosion** damage from combustion products. These include indirect methods using the pH and cond. measurements, and also direct methods that measure loss of metal on a target. These are discussed in this presentation. A recent development of **detg**. the **reliability** of electronic equipment when exposed to combustion products uses an interdigitated target and **measures leakage current** after the exposure. Data developed using this technique is presented and discussed. The combustion products were formed in the course of combustion of various plasticized and/or fireproofed polymeric materials. The study is of interest with respect to **evaluation** of **corrosion** of electronic equipment due to the **corrosivity** of smoke formed in the course of combustion of cable jacket and insulation materials.

L19 ANSWER 74 OF 287 CA COPYRIGHT 2002 ACS
AN 128:4384 CA
TI Development of **test** vehicles for **evaluating** plastic-encapsulant **reliability** and improving thermal conductivity of encapsulant materials
AU Enlow, Leonard R.; Swanson, Dale W.; Naito, Christine M.
CS Space and Missile Systems Sector, Autonetics & Missile Systems Division, Boeing, Anaheim, CA, 92803-3105, USA
SO Proceedings of SPIE-The International Society for Optical Engineering (1997), 3235(Proceedings 1997 International Symposium on Microelectronics, 1997), 314-321
AB Plastic-encapsulated microcircuits (PEMs) are proposed for use in military systems. PEMs reduce cost and eliminate long-lead items such as packages and lids. Encapsulant materials must be evaluated for compatibility with devices and fine-wire bonds, and elec. stability on deposited elements and integrated-circuit devices. **Reliability evaluations** in screen **tests** and various temp./**humidity**/bias environments are also essential prior to use in advanced packaging. Encapsulant **reliability evaluation** requires a **test** vehicle (MCM-C and MCM-L) to identify these key performance characteristics. Com. off-the-shelf parts that may be sensitive to encapsulant screening are transistor devices or PROM parts that can be **tested** for **leakage currents**, or programmed and verified. No complete multichip test vehicle, however, is available for use. An encapsulant test vehicle with three unpassivated resistor networks used in previous work was modified by substituting a Sandia ATC04 chip and a silver-comb-pattern array with varying feature sizes and using only a single nichrome-resistor network. Finally, a deposited comb pattern was added. The remaining single unpassivated resistor and a silver-comb pattern offer both a go/no-

go and quant. test for screening encapsulants. Use of the Sandia chip facilitates stress measurements on the die as well as thermal dissipation evaluation with resistance heaters on the chip. An industry-std. encapsulant, Hysol FP 4450, was modified by substitution of silica-coated aluminum nitride or boron nitride and spherical alumina fillers for the std. silica fillers. Other components in the material are a blend of epoxy resins and an arom. anhydride hardener. Exact filler selection and loading were optimized, balancing dispensability, wear, and flow characteristics. Control materials (Hysol FP 4450) and improved, thermally conductive versions were exposed to short-term screen **tests**, long-term temp. cycling, **humidity** cycling, and elevated temp. storage **testing**.

L19 ANSWER 77 OF 287 CA COPYRIGHT 2002 ACS
AN 127:87695 CA
TI Temperature-**humidity**-bias behavior and acceleration factors for nonhermetic uncooled InP-based lasers
AU Osenbach, J. W.; Evanosky, T. L.; Chand, N.; Comizzoli, R. B.; Krautter, H. W.
CS Lucent Technologies, Microelectronics, Optoelectronics Center, Breinigsville, PA, 18031, USA
SO ournal of Lightwave Technology (1997), 15(5), 861-873
AB The stability of uncooled InP-based laser diodes in humid ambients was studied. Nonhermetic devices were aged at 2 different temps. and **humidities** at a const. current and at 1 temp. and **humidity** at 6 different drive currents. For all nonhermetic devices failure occurred as a result of a large increase in the threshold current. The reverse **leakage current** for the failures did not increase when the threshold current increased, indicating that the change in threshold was a result of a change in reflectivity of 1 or both facets. The hermetic control group of devices aged under many of the same conditions showed a gradual increase in both the threshold current and slope efficiency. The median lifetimes as **detd**. by assuming a device was a **failure** when the threshold current increased by 50% was strongly dependent upon **humidity** temp. and drive current. The lifetime data was fit to and equation of the form lifetime exp(-Ea/kT) exp(-BRH[RH2]). The values of Ea and BRH were 0.52 eV and 4.9 × 10-4/%2, resp. The current drive data was fit to and expression of the form lifetime α exp(Ia Iop) where Ia as 0.09 h/mA. The lifetime dependence on current drive was modeled by assuming that the drive current caused a local temp. rise through thermal resistance. This local temp. rise then caused a decrease in the local **humidity** at the diode surface through an expression of the form %RHdiodeα exp{-5990[1/(Tr+Tambient)-1/Tambient]} where Tr is the local temp. rise due to thermal impedance. When the current dependent data was fit using this expression an activation energy, Ea and **humidity** exponent, B|rmRH, of 0.61 eV and 5.2 × 10-4/%2, resp., were detd. Since the current dependent data when modified for local thermal impedance yielded similar values of Ea and BRH to those **detd**. from the const. drive current multiple **humidity** and temp. data, the thermal impedance theory was correct. **Failure** mode **anal**. of the nonhermetic lasers which failed indicated that the failures were a result of either local facet coating defects (~10-20% of the devices failed for this cause) or facet coat delamination. The facet coat defects allow **moisture** to penetrate to the semiconductor facet. The **moisture** then oxidized the active region of the device and reduces the blocking layers of the device. This leads to degrdn. of the semiconductor in the active area of the facet and a loss of adhesion of the facet coat. The net result is a change in the facet reflectively as well as a change in the amt. of light scattering at or near the output facet. The combination of these 2 effects increases threshold and a decrease in slope efficiency. The facet delamination is a result of oxidn. that the exposed semiconductor

p-ohmic contact region of the device which is nor passivated with p-metals. The **moisture** oxidizes the p-ohmic contact region of the semiconductor. This causes a vol. change which imposes a stress on the facet coating. Apparently the stress exceeds the adhesion strength between the facet coat and the semiconductor. At this point, the facet coating delaminates. This leads to change in reflectivity and light scattering and eventually to a large shift in the threshold current and slope efficiency of the device. **Monitor** photodiode **failures** were also obsd. on some of the devices. The failure manifested itself as a large increase in dark current of the device. The data was evaluated with the same expression as was used for the laser aging data. The activation energy, Ea, is 0.4 eV. The **humidity** exponent BRH is 4.9 × 10-4/%2. The preliminary results on the reliability of nonhermetic SiOx passivated lasers are presented. Such lasers can be made with sufficient reliability for use in telecommunications application.

L19 ANSWER 81 OF 287 CA COPYRIGHT 2002 ACS
AN 126:212781 CA
TI **Leakage current** smoke **corrosivity testing** - comparison of cable and material data
AU Chapin, J. Thomas; Caudill, Loren M.; Gandhi, Pravin; Backstrom, Robert
CS Lucent Technologies, Bell Laboratories, Norcross, GA, USA
SO Proceedings of International Wire and Cable Symposium (1996), 45th, 184-193
AB This paper is the third in a series which presents elec. **leakage current measurements** on interdigitated **test** patterns exposed to smoke effluent from plastic materials and telecommunication cables. Six com. US and European cables were selected for testing. The **leakage current** behavior of each cable was **measured** and related to the fire performance rating of the cables. The cable **leakage currents** data are also compared to material data in order to investigate the effects of combustion of all combustible components in the cable. Co-combustion can affect the chem. and particulates of the smoke effluent which may also affect the **leakage current** results. This relationship is discussed. Supplemental data are also reported on the cable materials such as heat of combustion, ash content and elemental anal. in order to provide insight into the combustion and **leakage current** behavior.

L19 ANSWER 86 OF 287 CA COPYRIGHT 2002 ACS
AN 126:13467 CA
TI New hot carrier failure criterion for p-channel transistors based on transistor leakage currents
AU Doyle, B. S.; Mistry, K. R.
CS Digital Equipment Corp., Hudson, MA, 10749, USA
SO Solid-State Electronics (1996), 39(11), 1681-1682
AB Although hot carrier failure in very short channel (<0.35 μm) p-MOS transistors is often descried in terms of threshold voltage (Vt) shifts, a more meaningful hot carrier indicator for dynamic logic is the **leakage current**, Id.off (**measured** at Vd = - 3.6 V, Vg = -0.1 V). A new method for **detg**. the hot carrier **failure** time based on the leakage current is proposed here. This method has the advantage of being independent of the initial threshold voltage. A relation is proposed that links the leakage current to the effective length of the transistor. With this relation, it is possible to quickly screen for whether devices meet the hot carrier criterion, by simply **measuring** the **leakage current** and the effective channel length.

L19 ANSWER 90 OF 287 CA COPYRIGHT 2002 ACS
AN 125:183328 CA
TI Method and apparatus for **wafer-level prediction** of thin oxide **reliability**

IN Gabriel, Calvin T.; Subhash, Nariani R.
PA Vlsi Technology, Inc., USA
SO PCT Int. Appl., 36 pp.
PI WO 9623319 A2 19960801 WO 1996-US843 19960118
PRAI US 1995-376590 19950120
AB An IC wafer contg. thin oxide is fabricated with ≥1 pair of antenna structures having identical antenna ratios AR but different antenna plate areas. Each antenna structure includes 2 connected conductive plate regions, 1 plate formed over thick field oxide and the other plate formed over thin oxide on the IC. Because weak oxide **defects** occur somewhat uniformly throughout the thin oxide, a larger antenna structure will overlie more weak oxide **defects** than will a smaller antenna structure. If the wafer **test leakage current** across the larger antenna structure exceeds the **leakage current** across the smaller antenna structure, weak oxide is indicated because the **defect** is area-dependent. By contrast, charge-induced damage is substantially independent of the area of the antenna plates. Because the AR ratios are const., charge d. is const. in the antenna structure portions overlying the thin oxide. If the **test leakage current** on the wafer is substantially the same for each antenna structure, charge-damaged oxide is indicated because the damage is not area-dependent. If desired, test MOS devices may be fabricated whose gates are the plates formed over the thin oxide. **Defects** in the thin (gate) oxide may be identified by examg. the characteristics of the test MOS devices.

L19 ANSWER 95 OF 287 CA COPYRIGHT 2002 ACS
AN 124:329821 CA
TI Time-dependent dielectric degradation (TDDD) influenced by ultrathin film oxidation process
AU Kimura, Mikihiro; Ohmi, Tadahiro
CS Department of Electronic Engineering, Tohoku University, Sendai, 980, Japan
SO Jpn. J. Appl. Phys., Part 1 (1996), 35(2B), 1478-83
AB A complete hole-induced breakdown model suggests that the intrinsic oxide breakdown under optimal low-field operation lifetime is not a crit. limitation in thin oxide films (30-180 Å). Also, buildup of the oxide trapped charges and generation of the Si/SiO2 interface states during elec. stress, which is closely related to water-related bond breaking inside/at the interface of the amorphous thin oxide networks, decrease in a thin oxide film (~50 Å). On the other hand, elec. stress-induced **leakage current** (SILC) through the oxides is markedly increased in oxide films of around 50 Å thickness; also, the SILC is apparently dependent on the ultrathin film oxidn. process. The origin of SILC can be modeled by the Si-O weak/strained bonds inside the amorphous thin oxide films in contrast to the water-related bond-breaking model. Thus, the SILC phenomenon is a very important problem in the ultrathin oxide film reliability. Due to the need for a new **measure** of **wafer level reliability** to SILC, a time-dependent dielec. degrdn. (TDDD) method was developed for the **evaluation** of ultrathin oxide film **reliability**.

L19 ANSWER 100 OF 287 CA COPYRIGHT 2002 ACS
AN 124:161508 CA
TI In-situ **failure detection** in thick-film multilayer systems
AU Manca, J.; De Schepper, L.; De Ceuninck, W.; D'Olieslaeger, M.; Stals, L. M.
CS Inst. Mater. Res., Limburgs Univ. Cent., Diepenbeek, B-3590, Belg.
SO Eur. Symp. Reliab. Electron Devices, Failure Phys. Anal., 5th (1994), 309-13. Editor(s): Brydon, G. M. Publisher: National Technical Information Service, Springfield, Va.
AB By means of in-situ emf. **measurements**, **leakage current measurements**, and

impedance spectroscopy, it has been possible for the first time to detect spontaneous and force blistering in a thick-film multilayer during formation at high temps. Also, the occurrence of high-temp. shorts in Ag-dielec.-Ag multilayers under d.c. bias were detectable.

L19 ANSWER 107 OF 287 CA COPYRIGHT 2002 ACS
AN 123:114317 CA
TI Innovations in polymer arrester **moisture** sealing **testing**
AU Bennett, J. A.; Mackevich, J. P.; Member, Sr.; Mosso, R. J.
CS Raychem Corporation, Menlo Park, CA, USA
SO IEEE Trans. Power Delivery (1995), 10(1), 237-43
AB The vast majority of porcelain distribution arrester failures are the result of **moisture** ingress. Stds. lag technol. and do not currently address the unique design aspects of polymer arresters. Traditional sealing test methods cannot be run on polymer arresters because of lack of internal air space. A novel design **test** is proposed which involves sensitive interfacial **leakage current measurements** as the diagnostic. Samples are thermally cycled in water to produce thermal excursions and aging, while encouraging water ingress, should the sealing system be compromised. The proposed test is a modification of a protocol established for polymer insulators, which has been correlated to field service.

L19 ANSWER 110 OF 287 CA COPYRIGHT 2002 ACS
AN 122:303856 CA
TI Hot-carrier-induced off-state current leakage in submicrometer PMOSFET devices
AU Fang, Hao; Fang, Peng; Yue, John T.
CS Advanced Micro Devices, Inc., Sunnyvale, CA, 94088, USA
SO IEEE Electron Device Lett. (1994), 15(11), 463-5
AB Hot-carrier-induced off-state **leakage** (HCIOL) **currents** were successfully used as a new **monitor** in characterizing device **reliability**. HCIOL current increases drastically with reducing channel length, but the stress bias only affects the onset time of HCIOL current. For buried-channel PMOSFET's, only the HCIOL currents at the reverse measurement configuration were dominant. However, in surface-channel devices, HCIOL currents at both forward and reverse configurations became important. An empirical HCIOL current model was developed to quantify device lifetime as a function of channel length and stress voltage. Estd. lifetime results indicated that HCIOL current will impose a major limit on device reliability esp. for deep-submicrometer technol. and low power applications.

L19 ANSWER 119 OF 287 CA COPYRIGHT 2002 ACS
AN 118:259582 CA
TI Low temperature deposition of SiO2 and PSG using SiH4, N2O and phosphorous vapor for damage-free passivation of InP-based PIN diodes by plasma- and photo-assisted LPCVD
AU Riemenschneider, R.; DasGupta, N.; Schuetz, R.; Hartnagel, H. L.; Kraeutle, H.
CS Institute for High Frequency Electronics, TU Darmstadt, Merckstrasse 25, Darmstadt, D-6100, Germany
SO Appl. Surf. Sci. (1993), 69(1-4), 277-80
AB An improved deposition technique of phosphosilicate glass (PSG) for the passivation of InP was developed using a low-temp. plasma-enhanced CVD (PECVD). **Leakage-current measurements**, capacitance-voltage **analyses** (C-V curves), and deep-level transient spectroscopy (DLTS) were used compare this passivation technique with a commonly applied plasma CVD and a photo-assisted CVD of silicon oxide. Improvements regarding interface states and deep-level traps were achieved with a phosphorous vapor present during the

insulator growth. The measurement of leakage on a semi-insulating InP surface, which is very relevant for the reliability and performance of InP-based PIN diodes, provides **reliable** results to **detect** surface damage and material degrdn. The optimized plasma deposition of phosphosilicate glass at 300° with a low phosphorous concn. (<10 wt.% P) prevents surface leakage and does not show plasma damage.

L19 ANSWER 120 OF 287 CA COPYRIGHT 2002 ACS
AN 118:138059 CA
TI Manufacture of solid electrolytic capacitor
IN Nishijima, Yasuyo
PA ELNA Co., Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 3 pp.
PI JP 04225512 A2 19920814 JP 1990-414816 19901227
AB The title manuf. comprises dipping a capacitor element in H2O prior to forming a resin outer packaging to impregnate the element with H2O in a reduced pressure and **detg**. **current leakage** in an atm. within a predetd. time to **det**. **current leakage** increase due to **moisture** absorption.

L19 ANSWER 124 OF 287 CA COPYRIGHT 2002 ACS
AN 117:223823 CA
TI Minimization of parasitic currents in high-temperature conductivity measurements on high-resistivity insulators
AU Will, Fritz G.; Janora, Kevin H.
CS Gen. Electr. Co., Schenectady, NY, 12301, USA
SO J. Am. Ceram. Soc. (1992), 75(10), 2795-802
AB An exptl. setup and **novel measurement** technique are described which allow **reliable** cond. **measurements** to be made at conductivities as low as 10-17 Ω-1.cm-1 and temps. up to at least 1300°. This technique was used to measure the cond. of single-crystal alumina 400-1300° in a 10-7 torr (~1.3 × 10-5Pa) vacuum, equiv. to an O partial pressure of ~10-8 torr (~1.3 × 10-11 atm or ~1.3 × 10-6 Pa). Surface and gas-phase conductance are detd. as a function of temp., and the requirements for their minimization are described. A key requirement is a very low voltage between the vol. guard and the guarded electrode. The effect of **leakage currents** due to the sample fixture, elec. feed-through, and electronic instrumentation are also evaluated, and proper design features to make these effects negligible are outlined.

L19 ANSWER 131 OF 287 CA COPYRIGHT 2002 ACS
AN 116:185389 CA
TI Encapsulant for non-hermetic multichip packaging applications
AU Lin, A. W.; Wong, C. P.
CS AT and T Bell Lab., Murray Hill, NJ, 07974, USA
SO Proc. - Electron. Compon. Technol. Conf. (1991), 41st., 820-6
AB An encapsulant study was made that identifies a robust silicone material suitable for the multichip packaging (MCP) applications. The encapsulants were **tested** at 85°/85% relative **humidity** with DC bias and in-situ **leakage current monitoring**. A modified silicone encapsulant (MSE) was identified as the most promising material and was subjected to more in-depth studies. Test samples encapsulated with MSE were exposed to five selected chems. to study their chem. resistance. The samples were then subjected to temp.-**humidity**-bias (THB) **test** for **moisture** protection studies. In addn., the studies such as material formulation, adhesion, mech. protection and temp. cycling were conducted.

L19 ANSWER 136 OF 287 CA COPYRIGHT 2002 ACS
AN 115:137339 CA

TI Evaluation of polyimides as dielectric materials for multichip packages with multilevel interconnection structure
AU Lin, A. W.
CS AT and T Bell Lab., Murray Hill, NJ, 07974, USA
SO Proc. - Electron. Compon. Conf. (1989), 39th, 148-54
AB Using temp.-**humidity**-bias screening **test**, 9 com. polyimides were evaluated for applications in multichip packaging with a multilevel interconnection structure. DuPont PI2555 performed best under the **test** conditions, however, a slow increase of **leakage current** was obsd. in situ on the TiPdAu triple track test samples coated with PI2555. This performance was improved by modifying PI2555 with a proprietary additive, but the thermal stability of PI2555 was degraded by the additive. The dielec. const. of modified PI2555 was similar to the unmodified sample.

L19 ANSWER 141 OF 287 CA COPYRIGHT 2002 ACS
AN 114:33671 CA
TI The effect of volume resistivity on polymer electrical **leakage current measurements**
AU Troyk, Philip R.; Anderson, James E.
CS Illinois Inst. Technol., Chicago, IL, 60616, USA
SO Int. SAMPE Electron. Conf. (1989), 3(Electron. Mater. Processes), 969-82
AB The authors investigate the theor. **prediction** of elec. **leakage currents** for temp.-**humidity**-bias (THB) **tests**. An electrostatic finite element model was developed for triple-track and comb patterns. Using known values for vol. resistivity combined with a specific **test** pattern geometry, a **prediction** of **leakage currents** can be made. The model can be used to compute the **leakage current** for samples in which polymer-substrate interfacial currents are negligible thus **predicting leakage currents** for samples which would be expected to pass THB testing.

L19 ANSWER 142 OF 287 CA COPYRIGHT 2002 ACS
AN 114:7691 CA
TI Evaluation of polyimides as dielectric materials for multichip packages with multilevel interconnection structure
AU Lin, A. W.
CS AT and T Bell Lab., Murray Hill, NJ, 07974, USA
SO IEEE Trans. Compon., Hybrids, Manuf. Technol. (1990), 13(1), 207-13
AB Using a temp.-**humidity**-bias (THB) screening **test**, 9 com. polyimides were evaluated for applications of multichip packages with a multilevel interconnection structure. Among these polyimides, DuPoint PI2555 performed best under the test condition, i.e., 85°, 85% relative **humidity** and 180-V d.c. bias over 3-mil spacing. However, a slow increase of **leakage current** was obsd. in situ on the TiPdAu triple-track test sample coated with PI2555. This THB performance was improved by modifying PI2555 with a proprietary additive. However, the thermal stability of PI2555 was degraded by the additive. The dielec. const. of the modified PI2555 was detd. as 3.4 at 1 kHz, similar to that of PI2555.

L19 ANSWER 146 OF 287 CA COPYRIGHT 2002 ACS
AN 113:80558 CA
TI Enhanced **moisture** protection of electronic devices by ultrathin polyimide films
AU Burack, John J.; Legrange, Jane D.; Lin, A. W.
CS AT and T Bell Lab., Princeton, NJ, 08540, USA
SO IEEE Trans. Compon., Hybrids, Manuf. Technol. (1990), 13(1), 214-18
AB Thin films of polyimide which exhibit enhanced resistance to **moisture** were fabricated using the Langmuir-Blodgett (LB) technique. The adhesion strength of both LB and spin-coated films of several different polyimides,

deposited on fused silica, was measured by subjecting these films to steam or water, followed by a tape test, and monitoring changes in the UV spectra of the films, showing that the LB films of polyimide adhere better to fused silica than spin-coated films. In addn., water vapor transmission rate measurements through Kapton sheet coated by a monolayer of any of the polyimides show that a monolayer forms a **moisture** barrier, decreasing the water vapor transmission through the Kapton. Based on these results, the elec. performance of polyimide films was **tested** at 85°, 85% **humidity**, by **measuring leakage current** between conducting paths under 180-V bias, on samples which were coated with various combinations of LB and spin-coated polyimide films. Composite films of polyimide consisting of a LB monolayer, either underneath or on top of a thick, spin-coated film, exhibited superior elec. performance to either a spin-coated or LB film by itself. This may be explained by the improved adhesion and/or decreased water permeability of polyimide LB films.

L19 ANSWER 147 OF 287 CA COPYRIGHT 2002 ACS
AN 113:32688 CA
TI AC impedance **measurements** of **moisture** in interfaces between epoxy and oxidized silicon
AU Takahashi, Ken M.
CS AT and T Bell Lab., Murray Hill, NJ, 07974, USA
SO J. Appl. Phys. (1990), 67(7), 3419-29
AB In situ interfacial impedance measurements were used to study the effects of **moisture** at 80° on the interface between oxidized silicon and a diglycidyl ether of bisphenol A epoxy cured with diethylene triamine. Bulk impedance measurements follow Randles behavior; conduction in the bulk epoxy is ionic, and is diffusion-controlled at low frequencies. An addnl. conduction process between interfacial electrodes was obsd. even though a water layer does not condense in the interface. Through comparative use of linear network models, it is found that the "interfacial" conduction path represents distributed bulk conduction in the epoxy with displacement **current leakage** into the conductive silicon substrate through an interfacial capacitance. Both electrochem. and bulk coating properties jump at **humidities** near 70%, indicating greatly increased ionic mobility, coating permittivity, and interfacial capacitances. The permittivity and ionic mobility behavior suggest the formation of large water-swollen domains or highly elongated water clusters near the property jump threshold. Because **humidity** effects are resolved into bulk and interfacial components, interfacial impedance measurements appear to have great utility for the in situ study of transport and electrochem. properties of interfaces and coatings during environmental exposure.

L19 ANSWER 157 OF 287 CA COPYRIGHT 2002 ACS
AN 110:181576 CA
TI The influence of passivation layer on aluminum **corrosion** on simulated microelectronics circuit pattern
AU Wada, T.; Sugimoto, M.; Ajiki, T.
CS Qual. Lab., Matsushita Electron. Corp., Nagaokakyo, 617, Japan
SO J. Electrochem. Soc. (1989), 136(3), 732-5
AB The **corrosion** of thin Al is 1 of the important failure mechanisms in integrated circuits. Al **corrosion** and electrolytic **leakage current** were studied by temp.-**humidity**-bias **tests**. Two different passivation layers were investigated: a double layer of nondoped silicate glass (NSG) on phosphosilicate glass (PSG), and single layer of plasma-deposited SiN. Samples were prepd. with 3 different combinations of width/spacing: 2/2 μm (width/spacing), 4/4 and 12/6 μm, 2/2 and 4/4 μm patterns with a passivation layer on the stripes and a 12/6 μm pattern in which a part of

the passivation layer is etched to expose the Al stripe. Investigation of these patterns via temp.-**humidity**-bias **tests** leads to the following conclusions. With SiN passivation, cathodic Al **corrosion** did not occur on 2/2 and 4/4 μm patterns. On the other hand, with PSG + NSG passivation, cathodic **corrosion** occurred on 3 patterns. In 12/6 μm patterns with SiN passivation, the **leakage current** increased earlier than did that of 2/2 and 4/4 μm SiN passivated patterns. Thus, **leakage current** is conducted through the interface between the passivation layer and the plastic resin. In a special Al pattern in which a part of SiN passivation layer is etched to expose the stripe, local anodic **corrosion** was dominant. This anodic **corrosion** can be explained by the F in CF4/O2 plasma used for SiN etching.

L19 ANSWER 158 OF 287 CA COPYRIGHT 2002 ACS
AN 110:86436 CA
TI Testing of encapsulants for the protection of electronic components
AU Troyk, Philip R.; Conroy, David; Madigan, Michael
CS Illinois Inst. Technol., Chicago, IL, 60616, USA
SO Polym. Mater. Sci. Eng. (1988), 59, 497-501
AB A finite-element model was developed for **predicting** the value of **leakage currents** for the triple-track and comb patterns frequently used to **est. failure** rates for polymeric integrated circuits. The effects of substrate thickness and resistivity, as well as encapsulant thickness and resistivity could be modeled. The effect of a layer of condensed water on the surface of the encapsulant could also be investigated.

L19 ANSWER 159 OF 287 CA COPYRIGHT 2002 ACS
AN 109:191673 CA
TI Polymer-encapsulated microelectronics: mechanisms of protection and failure
AU Anderson, J. E.; Markovac, V.; Troyk, P. R.
CS Ford Motor Co., Dearborn, MI, 48121, USA
SO Mater. Res. Soc. Symp. Proc. (1988), 108(Electron. Packag. Mater. Sci. 3), 219-23
AB Mechanisms of electrochem. failure of polymer-encapsulated microelectronic devices due to surface **moisture** and surface impurities were studied by **measuring** the **leakage currents** on bare and siloxane-encapsulated Al combs as functions of temp., relative **humidity** (RH), and the presence of surface contaminants (NaCl, CaCl2, and sucrose). Under dry conditions (RH <1%), small **leakage currents** (1-10 pA) were obsd. which were insensitive to surface contamination levels. At RH >99%, surface-contaminated samples exhibited large **leakage currents** in the range 1-10 μA that were roughly proportional to the surface loading. Different surface contaminants produced **leakage-current** steps at specific RH values, corresponding to solid-to-satd. soln. transitions.

L19 ANSWER 170 OF 287 CA COPYRIGHT 2002 ACS
AN 107:166668 CA
TI Accelerated **corrosion testing** in pressure cooker at 130°
AU Burgess, J. F.; Yerman, A. J.
CS Corp. Res. Dev. Cent., Gen. Electr. Co., Schenectady, NY, 12301, USA
SO Proc. - Electron. Compon. Conf. (1986), 36th, 119-26
AB The results obtained from **moisture**-temp.-bias **testing** of power-MOSFET and Al triple-track devices at 130° and 85% relative **humidity** were examd. A variety of packaging techniques were tested varying from plastic encapsulation materials/methods to fully hermetic. Unprotected devices were tested as controls. The predominant failure mechanism is Al **corrosion** which was manifested initially as a **leakage current** increase and eventually as visually observable dissoln. of Al and eventual open circuits (in the case of Al triple-track pattern). The crit. role was examd. of surface

contamination in the **corrosion** process, particularly where condensed H2O films can form at the metal surface. The effectiveness of various plastic coating methods were viewed in the light of this concept. Al lead bonds are more susceptible to **corrosion** than expected. A no. of materials were identified that showed resistance to pressure-cooker conditions.

L19 ANSWER 175 OF 287 CA COPYRIGHT 2002 ACS
AN 106:225374 CA
TI Relationship between width and spacing of aluminum electrodes and aluminum **corrosion** on simulated microelectronic circuit patterns
AU Wada, T.; Sugimoto, M.; Ajiki, T.
CS QA Cent. Semicond. Group, Matsushita Electron. Corp., Nagaokakyo, 617, Japan
SO J. Electrochem. Soc. (1987), 134(3), 649-53
AB For fine pattern microelectronic circuits, there is a significant correlation between Al **corrosion** and the dimensions of the electrode. Electrolytic **leakage currents** and Al **corrosion** were studied using different combinations of width and spacing, 2/2 μm(width/spacing) and 4-4 μm, under temp.-**humidity**-bias **test** at 85-140°, 85%relative **humidity** and 0-150V. Electrolytic **leakage current** and 0.9 eV for Al **corrosion**. Activation energy values obtained from accelerated **tests** were 0.8 eV for electrolytic **leakage current** and 0.9 eV for Al **corrosion**. Also, the activation energy of Al **corrosion** was not affected by applied voltage. A paradoxical phenomenon was obsd. in that the **corrosion** resistance of the 2/2 μm pattern was greater than that of the 4/4 μm pattern when under an applied bias during exposure to the temp.-**humidity** environment. This phenomenon can be explained by crack formation in the passivation layer induced by Al **corrosion**.

L19 ANSWER 179 OF 287 CA COPYRIGHT 2002 ACS
AN 105:228555 CA
TI **Humidity testing** of silicone polymers for **corrosion** control of implanted medical electronic prostheses
AU Troyk, Philip R.; Watson, Michael J.; Poyezdala, James J.
CS Pritzer Inst. Med. Eng., Illinois Inst. Technol., Chicago, IL, 60616, USA
SO ACS Symp. Ser. (1986), 322(Polym. Mater. Corros. Control), 299-313
AB Adhesion tests were insufficient to quantify silicones for the **corrosion** control of electronic assemblies, and parameters such as material hardness might be of equal importance as the bond strength of the polymer to the protected assembly. Silane couplers did not enhance the **corrosion** control of silicone-encapsulated electronic devices probably due to water-sol. contaminants in the primers. Accelerated temp.-**humidity tests** on 72 interdigitated **test** substrates encapsulated with various silicone rubbers with or without surface primer treatment showed a strong dependence upon the material hardness in controlling **corrosion**. Elec. **leakage current measurements** combined with visual examn. were used as performance criteria for the encapsulants.

L19 ANSWER 189 OF 287 CA COPYRIGHT 2002 ACS
AN 104:27178 CA
TI Physical characterization of surface conductivity **sensors** in the aim of an absolute **moisture measurement** in electronic components
AU Kane, Didier; Gauthier, Roberty; Brizoux, Michel; Perdrigeat, Jacky
CS Thomson-CSF, Orsay, Fr.
SO Proc. - Electron. Compon. Conf. (1984), 34th, 441-7
AB A phys. interpretation is proposed for the I(T) curve which gives the evolution of the **leakage current** I of a surface cond. **moisture sensor** vs. temp. The interpretation makes use of a multimol. layer phys. adsorption

model. Chemisorptive phenomena during the adsorption phase can be neglected. The relationship of the I(T) curve to dew-point **measurements** for **detn.** of abs. **humidity** is discussed.

L19 ANSWER 202 OF 287 CA COPYRIGHT 2002 ACS
AN 100:176996 CA
TI **Humidity sensors**
PA Matsushita Electric Industrial Co., Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 6 pp.
PI JP 59004113 A2 19840110 JP 1982-114588 19820630
AB The **humidity sensors** are made by anodic **oxidn.** of metals (e.g., Ta), coating the oxide layer with semiconductors (e.g., MnO2), coating the semiconductor layer with C, painting with 2 Ag **electrodes**, and irradn. with far IR under vacuum. They have high reliability even after long storage.

L19 ANSWER 203 OF 287 CA COPYRIGHT 2002 ACS
AN 100:176994 CA
TI **Humidity sensors**
PA Matsushita Electric Industrial Co., Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 6 pp.
PI JP 59005619 A2 19840112 JP 1982-114844 19820701
AB The **humidity sensors** are made by anodic **oxidn.** of metals (e.g., Ta), coating the oxide layer with semiconductors (e.g., MnO2), and depositing 2 **electrodes** (made of, e.g., cellulose diacetate contg. dispersed Ag powder) on the semiconductor layer. Their electrostatic capacitance-relative humidity relation is linear.

L19 ANSWER 205 OF 287 CA COPYRIGHT 2002 ACS
AN 100:141311 CA
TI **Humidity sensors** with high sensitivity and stability
PA Omron Tateishi Electronics Co., Japan
SO Jpn. Kokai Tokkyo Koho, 4 pp.
PI JP 59004102 A2 19840110 JP 1982-114543 19820630
AB In **humidity sensors** fabricated by forming **humidity-sensing** resistor layers between a pair of **electrodes** on insulating substrate plates, the **humidity-sensing** resistor layers contain a V compd. 3-30 mol% (e.g., VC, VN, V2O5, V2O3, VO2, SrV2O6, MnV2O6, FeV2O6) as oxidn. catalyst. The **humidity sensors** have high sensitivity in **humidity detn.**, and no addnl. cleaning process is required. Thus, a paste of LiPbNbO4 60, MnCr2O4 20, and VC 20 mol% was screen-printed on the gaps between 2 comblike **electrodes** formed on a ceramic substrate plate, fired at 900-1200°, and aged at high temp. and high humidity after attaching 2 lead wires to make a **humidity sensor**. Its resistance was 1.10 × 106, 7.2 × 104, and 7.4 × 103 Ω at 30, 60, and 90% relative humidity, resp.

L19 ANSWER 206 OF 287 CA COPYRIGHT 2002 ACS
AN 100:130673 CA
TI The relationship between **moisture** resistance and epoxy molding compounds in integrated circuits
AU Nakagawa, Osamu; Sasaki, Ikuo; Hamamura, Hideo; Banjo, Toshinobu
CS Kita-Itami Works, Mitsubishi Electr. Corp., Itami, Japan
SO J. Electron. Mater. (1984), 13(2), 231-50
AB The influence of epoxy molding compds. on Al **corrosion** in a Pressure Cooker **Test** was investigated by means of a monitor chip encapsulated in a dual-in-line package. The **monitor** chip is composed of a **leakage-current-measuring** part and a **corrosion-measuring** part. The **moisture** resistance was improved by proper selection of the internal release agent and coupling agent, and by decreasing the stress in the epoxy molding compd.

L19 ANSWER 208 OF 287 CA COPYRIGHT 2002 ACS
AN 100:87771 CA
TI Anode-oxidized aluminum **humidity sensor**
PA Hokuriku Electric Industry Co., Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 4 pp.
PI JP 58189548 A2 19831105 JP 1982-70520 19820428
AB The sensor is an anodic-oxidized Al layer over a pair of comb-shaped **electrodes** on an elec.-insulating plate with a water-permeable covering layer (thickness 500-2000 Å) of elec.-conductive metal, e.g., Au, Ag, Cr, or Ni. Thus, an Al layer (thickness 5000-7000 Å) was formed by vapor deposition on a Ta-sputtered Al2O3 plate (10 × 15 × 0.6 mm) over a pair of comb-shaped **electrodes**. The Al layer was anode-oxidized in dil. aq. H2SO4 or (COOH)2, washed by water, stabilized by heating 2 h at 300-350°, and coated with Au (thickness 2000 Å) by vapor deposition. The Au that penetrated to near the **electrodes** was removed by heating <10 s by applying 130-150 V between the **electrodes**.

L19 ANSWER 214 OF 287 CA COPYRIGHT 2002 ACS
AN 100:53661 CA
TI Cathode-oxidized aluminum **humidity sensor**
PA Hokuriku Electric Industry Co., Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 7 pp.
PI JP 58179348 A2 19831020 JP 1982-61132 19820414
AB The multilayer sensor has a cathode-oxidized Al coating over a pair of comb-shaped Ta **electrodes** on an elec.-insulating plate, a surfactant layer of polyoxyethylene alkylphenyl ether, and a water-permeable film of Au, Ag, Ni, or Cr (thickness 500-2000 Å) at the top. Thus, a Ta layer (thickness 2000 Å) was formed by sputtering and etched to a pair of comb-shaped **electrodes** which were covered by Al (thickness 5000-7000 Å), and cathode-oxidized with dil. H2SO4. Au was vapor deposited on the surface of the element to the thickness 1000 Å as a nonoxidizable and H2O-permeable layer, coated with 0.1-1 vol.% polyoxyethylene alkylphenyl ether, and dried. The elec. resistance of the element was ~10 kΩ.

L19 ***ANSWER 219 OF 287*** CA COPYRIGHT 2002 ACS
AN 97:64838 CA
TI A surface conductivity **moisture monitor** for hermetic IC packages
AU Lowry, Robert K.
CS Prod. Div., Harris Semicond., Melbourne, FL, 32901, USA
SO NBS Spec. Publ. (U. S.) (1982), 400-72, 64-75
AB An in-situ surface cond. sensor for measuring water content of hermetic integrated-circuit (IC) package cavity ambients is described. The sensor is a 50 × 95-mil chip whose surface consists of an interdigitated pattern of Al stripes on SiO2. The chip is mounted and wire bonded as a **test** vehicle into the package configuration whose **moisture** content is to be **detd**. The hermetically sealed specimen package is cooled in a temp. bath with 50 V d.c. applied to the sensor. As **moisture** condenses onto the **sensor** surface, the **leakage current** of the metal pattern rises. The temp. value of the **leakage current** peak represents complete condensation of all available H2O vapor, and this is nomog. converted to ppm H2O content. Sensor performance is evaluated via correlation expts. with mass spectroscopy and vol.-effect sensors. Use of the sensor to est. levels of metal ions within the package cavity is also described.

L19 ***ANSWER 222 OF 287*** CA COPYRIGHT 2002 ACS
AN 96:182804 CA
TI A **moisture** protection screening **test** for hybrid circuit encapsulants
AU Mancke, R. G.

CS Bell Teleph. Lab. Inc., Allentown, PA, 18103, USA
SO IEEE Trans. Compon., Hybrids, Manuf. Technol. (1981), CHMT-4(4), 492-8
AB An empirical comparative screening test for polymeric encapsulants was described and used to indicate how well different materials prevent unwanted **leakage currents** between closely spaced biased metal lines in hybrid integrated circuits. The screening test circuit, test procedure, and test conditions are described. This test and measurement equipment were developed earlier by N. L. Sbar and R. P. Kozakiewicz (1977-9). Data for two silicone coatings and one epoxy coating were compared with data for DC 3-6550 RTV. Results are also shown for layers of two different polymer coatings. The coatings of the same general polymer type varied considerably in performance in this screening test.

L19 ANSWER 223 OF 287 CA COPYRIGHT 2002 ACS
AN 96:153905 CA
TI Cleaning processes for high voltage circuits with soldered chip carriers
AU Schlough, Susan D.; O'Connell, Edward F.
CS Bell Lab., Allentown, PA, 18103, USA
SO Int. J. Hybrid Microelectron. (1981), 4(2), 27-38
AB To develop suitable cleaning techniques for use on high-voltage hybrid integrated circuits, assembled testers were cleaned with one of several processes prior to encapsulation with RTV, with the following results: (1) a process utilizing Freon TMC for flux removal, followed by pre-encapsulation cleaning including 3 min in H2O2, is an effective cleaning method for ceramic circuits to be operated at high voltages; (2) a cleaning process utilizing Loncoterge 446 results in effective removal of both flux and ionic contaminants, but accelerated aging performance indicates a need for better methods of eliminating detergent residues after cleaning; (3) an obsd. difference in **leakage currents** for circuits with and without chip carriers is due to thinner RTV under the chip carriers, rather than to poorer under-chip-carrier cleaning. **Reliability testing** at accelerated conditions of 85°/85% relative **humidity** and 1000 V was performed on double-sided circuit testers with a chip-carrier soldered on each side. Cleaning effectiveness was **detd.** by **measuring leakage currents** on fine-line conductor patterns located under the chip carriers. Failure data resulting from this expt. were compared with data from deliberately contaminated samples which were fluxed, soldered, cleaned, and then analyzed with a custom-built ionic contamination detection system.

L19 ANSWER 225 OF 287 CA COPYRIGHT 2002 ACS
AN 95:213922 CA
TI A **moisture** protection screening **test** for hybrid circuit encapsulants
AU Mancke, R. G.
CS Bell Telephone Lab., Inc., Allentown, PA, 18103, USA
SO Proc. - Electron. Compon. Conf. (1981), 31st, 119-25
AB An empirical, comparative screening test for polymeric encapsulants shows how well they would prevent unwanted **leakage currents** between closely spaced, biased metal lines in integrated circuits and hybrid integrated circuits. It is not a **reliability test**. The screening test circuit, test procedure, and test conditions are described. This test and measurement equipment were developed earlier by N. L. Sbar and R. P. Kozakiewicz (1977; 1979). Data for 2 silicone coatings and 1 epoxy coating are compared with data for Dow Corning 3-6550 RTV. Results are also shown for layers of 2 different polymer coatings. Coatings of the same general polymer type can vary quite dramatically in performance in this screening test.

L19 ANSWER 241 OF 287 CA COPYRIGHT 2002 ACS
AN 85:55173 CA

TI Bias-**humidity** performance of encapsulated and unencapsulated titanium-palladium-gold thin film conductors in an environment contaminated with chlorine
AU Sbar, Neil L.
CS Bell Teleph. Lab., Inc., Allentown, Pa., USA
SO Proc. - Electron. Components Conf. (1976), 26, 277-84
AB Encapsulated and unencapasulated Ti-Pd-Au thin-film conductors on Al2O3 substrates were biased in an 85°, 80% relative **humidity** environment contaminated wth 1.7 ppm Cl. The conductors were 3 mils wide, and oppositely biased conductors were spaced 3 mils apart. The encapsulant was an RTV silicone rubber. During exposure to the **corrosive** environment, in-situ **leakage currents** were **measured** periodically for each conductor circuit. **Leakage currents** for the unencapsulated specimens increased with time, and many were shorted after ~400 hr. There was no increase in **leakage currents** for the encapsulated conductors. At the end of the test, selected specimens were examd. by using a light microscope and a scanning electron microscope with x-ray capability. No metal migration was obsd. on the encapsulated samples. The unencapsulated conductors showed dendritic growth between the electrodes; x-ray anal. showed the growths to consist of Au and Pd. The RTV silicone encapsulant prevented high **leakage currents** and subsequent metal migration on Ti-Pd-Au conductor specimens exposed to the moist Cl environment under bias. Unencapsulated samples were degraded rapidly under the same conditions; the main failure mechanism was metal migration.

L19 ANSWER 257 OF 287 CA COPYRIGHT 2002 ACS
AN 72:126487 CA
TI Performance of epoxy molding compounds on DIP integrated circuits
AU Johnson, George; Benham, Ronald
CS Hysol Div., Dexter Corp., Olean, N. Y., USA
SO Mater. Processes 70's, Nat. SAMPE (Soc. Aerosp. Mater. Process Eng.) Symp. Exhib., 15th (1969), 531-7
AB A test method was developed to provide a comparative **evaluation** of epoxy molding compd. **moisture** performance on DIP integrated circuits. Data are presented displaying relative **moisture** protection provided by these epoxy compds. as detd. by evaluation of encapsulated dummy integrated circuits. Correlation of the dummy results with actual live device performance in these materials confirmed the value of the proposed test method. The epoxy molding compds. were either mineral filled or mineral filled-fiber reinforced.

L19 ANSWER 259 OF 287 CA COPYRIGHT 2002 ACS
AN 71:117504 CA
TI Encapsulation of integrated circuits
AU White, Malcolm Lunt
CS Bell Teleph. Lab., Inc., Allentown, Pa., USA
SO Proc. IEEE (1969), 57(9), 1610-15
AB Integrated circuits mounted on ceramic substrates must be protected from **moisture** and from mech. damage by an encapsulation system which must have the same long-term stability as the device itself. Beam-lead Si nitride protected circuits are subjected to >300° long-term aging as well as to high-temp. steam to accelerate failures; thus, encapsulants must have the same stability. A silicone-based encapsulation system which meets these rigid requirements is described. A no. of resins and rubbers have been **evaluated** for their ability to maintain low **leakage currents** under high **humidity** conditions by **measurement** of the leakage on coated metallized ceramics under both high **humidity** and liq. water environments. An accelerated aging program was carried out to establish the long-term

stability of these coating systems from the standpoint of their **moisture**-protecting abilities. The extrapolated lifetime of the silicone coatings is about the same as that established for the integrated circuits at their operating temp. From consideration of published permeability data and the results obtained in this study, it appears that the mechanism of protection against **moisture** is the inactivation of sites on the surface where water can adsorb or condense to form a continuous film of water which could lead to elec. **leakage currents** on either the device or substrate surfaces. The best protection is thus afforded by those materials that either chem. react with the surface or are strongly adsorbed at the sites where water would normally condense.

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